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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
FOONG, SUK SAN

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 03/31/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/910,914	Applicant(s) AHN ET AL.	
	Examiner Suk-San Foong	Art Unit 2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-45* is/are pending in the application.

4a) Of the above claim(s) *31-45* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 11-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-6, 9-13, 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jiang et al. ('880) in combination with Lopatin et al. ('954), AAPA (Applicant's Admitted Prior Art and Kaloyeros et al.

Jiang et al., Lopatin et al. and AAPA are relied on for the teachings discussed in the rejections of paragraph 10 of the Office Action mailed on 11/5/02 and as follows.

The combination process does not teach that copper is selectively deposited using a low-temperature metal-organic chemical vapor deposition method.

Kaloyeros et al. discloses a method of selectively depositing copper in vias or openings for multilevel metallization for integrated circuits using low-temperature metal-organic chemical

vapor deposition at 300-400°C in atmosphere of pure H_2 or Argon from β-diketonate precursor bis(6,6,7,7,8,8,8-heptafluoro-2,2-dimetyl 1-3,5-octanedion) copper (II) (Abstract).

It would have been within the scope to one ordinary skill in the art to combine the teachings of Kaloyeros et al. with the combination process because it would enable formation of copper layer 110 of the combination to be performed and obtain further advantage of copper film having uniform, continuous and low resistivity (Kaloyeros et al., p. 84, 1st paragraph).

4. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jiang et al. ('880) in combination with Lopatin et al. ('954), Applicant's Admitted Prior Art (AAPA) and Kaloyeros et al. as applied to claims 1-6, 9-13, 15 and 16 above, and further in view of Farrar ('931).

The rejection is maintained as stated in paragraph 11 of the Office Action mailed on 11/5/02.

5. Claims 14, 17-20, 23 and 28-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jiang et al. ('880) in combination with Lopatin et al. ('954), Applicant's Admitted Prior Art (AAPA), Shacham-Diamand et al. and Liu et al. ('962).

Jiang et al. teach the method of forming copper interconnect layers for semiconductor devices which includes forming an interlevel dielectric 102 (ILD) and intermetal dielectric 104 (IMD) layers comprise of same or differing low-k material such as hydrogen silesquioxane (Paragraph [0018]), etching trench 120 in IMD 104 (Paragraph [0019]), then depositing barrier layer 106 by atomic layer deposition on the surface of IMD 104 and trench 120 (Fig. 2C),

depositing copper layer 110 over trench 120 and IMD 104 (Fig. 2D), and removing portions of the copper layer 110 and barrier layer 106 by CMP (Paragraph [0024]).

Jiang et al. does not list methylsilsesquiazane as one of the low-k dielectric materials nor teach patterning low dielectric constant layer to form openings in low-k dielectric layer by exposing to electron beam or ultra violet light and etching by tetra-methyl-ammonium hydroxide.

APPA discloses the method of forming low dielectric constant copper interconnects which includes patterning low dielectric constant layer, methylsilsesquiazane with dielectric constant of 2.7, through electron beam (EB) and/or ultraviolet (UV) irradiation and further developed by tetra-methyl-ammonium hydroxide (TMAH) to form vias (Instant page 8, line 13 to Instant page 9, line 11).

It would have been within the scope to one ordinary skill in the art to combine the teachings of AAPA with Jiang et al. because it would enable formation of openings through low dielectric constant layer and obtain further advantage of eliminating both photoresist and dry etching process steps.

The combination process does not disclose that the barrier layer is formed using tungsten nitride.

Lopatin et al. teach the method of forming metal interconnect which includes providing trench region 220 (Figs. 2 and 3) in low dielectric constant layer (Col. 5, lines 37-39), then forming tungsten nitride barrier layer 401 over trench region 220 (Col. 5, lines 20-25) using ALD (Col. 4, lines 31-32) at a temperature between 373°K to 673°K (Col. 4, lines 42-45), forming copper pre-seed layer 402 (Col. 5, lines 41-45, and Col. 6, lines 6-10), then forming

copper seed layer 403 (Col. 6, lines 30-54), then depositing cooper layer 404 by chemical vapor deposition (Col. 6, lines 63-65), and removing excess copper layer 404, seed layer 403, pre-seed layer 402 and barrier layer 401 through CMP (Fig. 9, and Col. 6, lines 65-67).

It would have been within the scope to one ordinary skill in the art to combine the teachings of Lopatin et al. with the combination process because it would enable formation of barrier layer 106 in trench 120 of the combination process to be performed and obtain further advantage of providing excellent adhesion to the underlying low dielectric material (Lopatin et al., Col. 5, lines 37-39).

The combination process does not disclose removing portions of tungsten nitride layer above surface of low-dielectric constant layer by chemical-mechanical polishing prior to depositing copper layer.

Liu et al. teaches a method of forming damascene structure for semiconductor devices which includes forming opening 160 in low dielectric constant layers 110, 130 (Col. 5 lines 45-52, and Fig. 2C), subsequently depositing barrier layer 170, comprised of material such as tungsten nitride, and seed copper layer 180 in opening 160 (Col. 6, lines 31-44, and Fig. 3A), then removing a portion of barrier layer 170 and seed copper layer 180 formed above the surface of low dielectric constant layer 130 (Col. 6, lines 48-54 and 63-66, and Fig. 3D), subsequently depositing copper layer 200 in opening 160 using electroless deposition method (Col. 7, lines 10-20, and Fig. 3E), and then removing portions of copper layer 200 (Col. 7, lines 21-37, and Fig. 3F).

It would have been within the scope to one ordinary skill in the art to combine the teachings of Liu et al. with the combination process because it would removal of portions of

barrier layer 106 prior to copper layer deposition in the combination process and obtain further advantage of reducing amenability to dishing (Liu et al., Col. 4, lines 4-6).

The combination process does not teach forming copper layer by electroless deposition using contact displacement method at room temperature.

Shacham-Diamand et al. discloses a method of forming copper film for integrated circuit metallization on a surface of a barrier layer through an electroless deposition process using a contact displacement method at room temperature (p. 51, 4th paragraph).

It would have been within the scope to one ordinary skill in the art to combine the teachings Shacham-Diamand et al. with the combination process because it would enable formation of copper layer 110 in trench 120 of the combination process to be performed and obtain further advantage of the low cost of the tools and materials and high throughput of the process (Shacham-Diamand et al., p. 48, 1st paragraph).

6. Claims 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jiang et al. ('880) in combination with Lopatin et al. ('954), Applicant's Admitted Prior Art (AAPA), Shacham-Diamand et al. and Liu et al. ('962) as applied to claims 14, 17-20, 23 and 28-30 above, and further in view of Farrar ('931).

The combination process does not teach forming low dielectric constant layer to a thickness of about 6,000 Angstrom to 20,000 Angstroms by spin coating.

Farrar discloses the method of forming trenches and vias from low dielectric constant materials which includes providing metal layer 52 as lower metal interconnect layer (Paragraph [0034]), sequentially depositing low dielectric constant layer 55 and another low dielectric

constant layer 57 (with both having dielectric constants lower than 4.0) by using spin coating process to a thickness of about 2,000 Angstrom to15,000 Angstrom (Paragraphs [0036]-[0038]), subsequent forming via 65 and trench 67 (Fig. 12), forming barrier layer 72 in via 65 and trench 67 (Fig. 13, or Paragraph [0045]), then depositing copper 80 to fill in both via 65 and trench 67 by CVD (Paragraph [0048]), and removing copper 80 above the surface of layer 57 by CMP.

It would have been within the scope to one ordinary skill in the art to combine the teachings of Farrar and the combination process because it would enable the step of forming low constant dielectric layers 102 and 104 of the combination process to be performed and obtain further advantage of eliminating etch stop layers and reduce the number of fabrication steps.

7. Claims 24-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jiang et al. ('880) in combination with Lopatin et al. ('954), Applicant's Admitted Prior Art (AAPA), Shacham-Diamand et al. and Liu et al. ('962) as applied to claims 14, 17-20, 23 and 28-30 above, and further in view of Kaloyeros et al.

The combination process does not teach the step as recited in claim 24, lines 1-2.

The combination process does not teach the step as recited in claim 25, lines 1-2.

The combination process does not teach the step as recited in claim 26, lines 1-3.

The combination process does not teach the step as recited in claim 27. lines 1-3.

Kaloyeros et al. discloses a method of selectively depositing copper in vias or openings for multilevel metallization for integrated circuits using low-temperature metal-organic chemical vapor deposition at 300-400°C in atmosphere of pure H_2 or Argon from β-diketonate precursor bis(6,6,7,7,8,8,8-heptafluoro-2,2-dimetyl 1-3,5-octanedion) copper (II) (Abstract).

It would have been within the scope to one ordinary skill in the art to combine the teachings of Kaloyeros et al. with the combination process because it would enable formation of copper layer 110 of the combination to be performed and obtain further advantage of copper film having uniform, continuous and low resistivity (Kaloyeros et al., p. 84, 1st paragraph).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suk-San Foong whose telephone number is 703-305-0383. The examiner can normally be reached on Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 (7724, 3431, 3432).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

SF
March 20, 2003

George Fourson
Primary Examiner
Art Unit 2823